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IMPLEMENTATION OF LOW POWER EXPLICIT PLUSE- TRIGGERED FLIPFLOP BASED ON SIGNAL FEED THROUGH SCHEME

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ABSTRACT

Power consumption is a key design factor in many circuits. We can say low power concept is a skeleton of electronic industry. The requirement of low power is for consideration of power dissipation and the greatest challenge regarding area and circuit performance. A low power flip-flop design structure is explicit type pulse, trigger and a modified single phase clock is used for signal feed through the scheme. Pulse-triggered FF (PFF) is a single-latch structure that is more advantageous than the conventional transmission gate (TG) and master–slave based FFs in high-speed applications. In this work we have implemented various edges triggered flip-flop and studied their behaviour. We then proposed an Efficient P-FF design solves the long discharging path problem in case of conventional explicit type pulse-triggered FF (P-FF) and achieves better speed and power performance. Based on post-layout simulation results using Micro wind CMOS 90-nm technology, the Efficient P-FF design outperforms the conventional P-FF design in data-to-Q delay. In the meantime, the performance edges on power metrics respectively. Various simulation results based on CMOS 90-nm technology reveals that the Efficient P-FF design is power efficient when the pulse generator is shared with multiple FF's. A better D-to-Q Delay is achieved. Both cadence virtuoso (90 nm technology) and micro-wind version 3.0.0 were used in the study and implementation of the circuits in this work

KEYWORDS: PFF, Flip-Flop, SDFF, HLFF

INTRODUCTION

Today's technologies make possible powerful computing devices with multimedia capabilities. Consumers' attitudes are gearing towards better accessibility and mobility. Their desire has caused a great demand for an ever increasing number of portable applications requiring low-power and high throughput. Low power VLSI systems are exponentially used in mobile devices, instrument for biomedical, signal and systems. In general purpose electronics systems such as personal computers, cellular phones, or handheld computers, i.e., tablets PC, we may find numerous Integrated Circuits (IC), placed together with discrete components on a Printed Circuit Board (PCB). The integrated circuits appearing in this figure have various sizes and complexity. The circuit consists of a microprocessor which is called as the heart of the system that is only chip which includes millions of transistors. The push for smaller size, reduced power supply consumption and enhancement of services, has resulted in continuous technological advances, with possibility for ever higher integration For example, notebook and handheld computers are now made with competitive computational capabilities as those found in desktop machines. Equally demanding are personal communication applications in a pocket-sized device. In these applications, not only voice, but data as well as video are transmitted via wireless links. It is important that these high computational capabilities are placed in a low-power, portable environment. The weight and size

of these portable devices are determined by the amount of power required. The battery lifetime for such products is crucial. Hence, a well-planned low energy design strategy must be in place. As the density of the integrated circuits and size of the chips and systems continues to grow, it becomes more and more difficult to provide adequate cooling for the systems. In addition to heat removal, there are also economic and environmental issues for low power development.

STUDY OF DIFFERENT CONFIGURATIONS OF FLIP FLOPS

Pulse Triggered Flip-Flop

Pulse-triggered Flip-Flop (P-FF) has been considered as more popular to the conventional master –slave based FF which is used in high speed operation. The P-FF circuit also advantage to reduce the power consumption of the clock tree system. In case of P-FF consist of a latch for storing the data and a pulse generator for generating strobe signals. If the triggering pulse generated on the transition (0 to 1) edges of clock, i.e. called as positive edge triggered flip-flop. The complexity of the circuit is simplified only once, which is used in conventional master-slave configuration. Generally a P-FF having negative set-up time and having time borrowing clock cycle boundaries that's why the P-FF are less sensitive to clock jitter. The greatest advantage is that the pulse generation to delicate pulse width control and configuration of clock distribution of the network.

Classification of Pulse Triggered Flip-Flop

Depending on the method of pulse generation, the pulse-triggered flip-flops can be classified into two types, implicit and explicit, and this classification is due to the pulse generators they use. In case of implicit type of p flip-flop the pulse generated only inside. Just an example SDFF (semi dynamic flip-flop), HLFF (hybrid latch flip-flop) and IP-DCO (implicit pulse data close to the output).In case of explicit type of flip-flop, the pulse is generated outside. The examples are ep-DCO (explicit pulse data close to the output) [2]. No explicit pulse signal is generated in the case of implicit type of flip-flop and the pulse generator is a type of latch design. The pulse generator and latch are separate in case of explicit type of P-FF. If we consider in case of power consumption implicit pulse generation having a greater advantage rather than explicit, but the main demerit is the longest discharging path problem which leads to inferior timing characteristics [1]. In case of explicit pulse generation the logic separation of the latch design gives the unique speed advantage. If the pulse generator shares the input group of flip-flops, then the complexity of the circuit and power consumption effectively reduced [3].

The flip-flop we have implemented in VHDL programming, we got the block and an RTL schematic diagram of pulse trigger. After completion of schematic we have drawn the circuit diagram of the pulse trigger circuit by using cadence and got the desired output. After getting the output we have implemented the pulse trigger in various circuits where the circuit diagram. Then the same circuit drawn in micro wind tool and gave input pulse at an instance of time and got the timing diagram which has shown in chapter results and simulation part. From this timing diagram, we have extracted the data setup time, hold time, maximum current and power. All the parameter we have listed in a table *(refer chapter-4, table-1).*

Then all circuit diagrams converted to lay out diagram by using DSCH simulator where the. Then we have to see the value of λ then we have to calculate each block and find out the length and breadth then we found out the area. The various circuits have calculated area then we have put each circuit area in each circuit (table 2)

From layout diagram, if we simulate then we found power, delay, maximum current then all the figure and the parameters are tabulated (table 3)

Then we multiply the power with delay and will get the power delay product which is shown in bar chat.

Explicit-Pulsed Data-Close-to-Output Flip-Flop (EP-DCO)

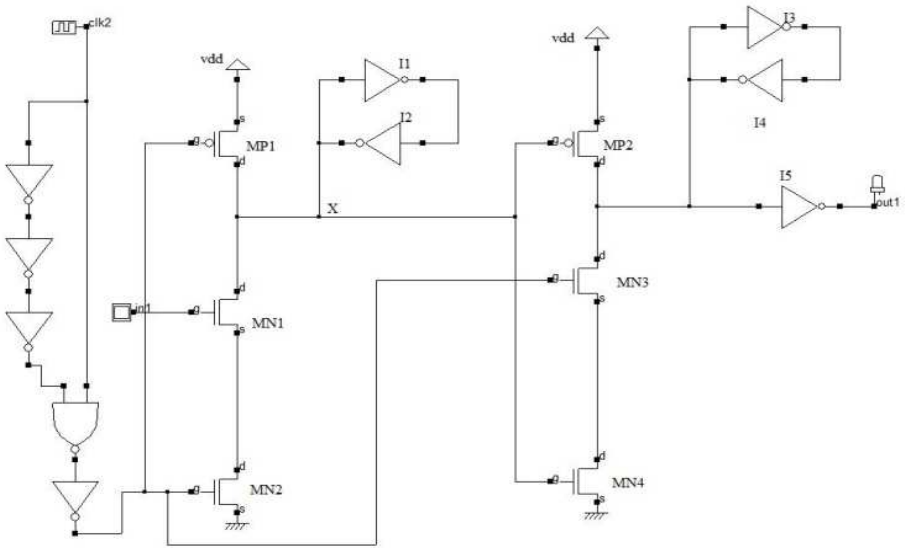

Figure 1: Circuit in EP-DCO

This circuit design contains pulse generator, which is pulse NAND-logic based and latch design is there having semi dynamic true single phase clock (tspc). In case of P-FF design, I3 and I4 inverters are used to latch the data and I1 and I2 inverters are used to hold the internal node x. Figure 1 shows the schematic of the Explicit-Pulse Data-Close-to-Output flip-flop (ep-DCO), which is considered as one of the fastest flip-flops due to its semi dynamic nature. It has the pulse generator of the Explicit-Pulse Data-Close-to-Output EP-DCO flip-flop. In this circuit the three inverters are having own delay which is used to generate the pulse at the double edge of clock. There are two stages in case of ep-DCO and the 1st stage is called as dynamic and the 2nd stage is treated as static. Here, the clock pulse is used drive three transistors-MP1, MN2 and MN3.The input data is cHearcted to MN1 and the circuit captures the data through MN1.When the flip-flop is transparent, the input data propagates to the output, after the transparent period, MN2 and MN3 will turn off because of the low voltage of the pulse, at the same time, point X change to the high voltage because that MP1 is on at this time. So MP2 is off after the transparent period. Hence, any change in the input cannot be passed to the output. Now, we begin to analyze the disadvantages of ep-DCO. The internal node X will be charged or discharged at every clock cycle, especially when the input data does not change, a lot of power is consumed at this point. [1] [3]. We have also drawn diagram in cadence.

Conditional D Flip-Flop

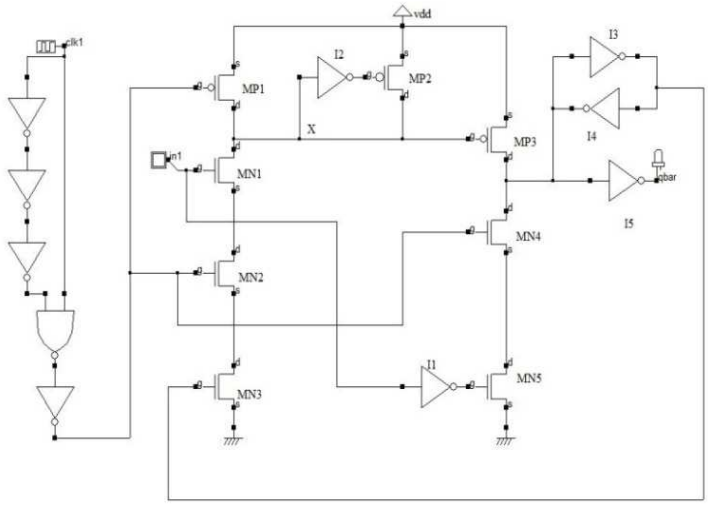

Figure 2: Circuit in CDFF

When the input is stable and high, then the extra switching activity is eliminated by controlling the discharging path that's why the circuit name is called as conditional discharge technique. An extra NMOS transistor controlled by the output signal Q feedback is employed so that no discharge occurs if the input data remains "1". Power consumption in this design is high and the discharging path delay is more [1] [3]. In conditional flip-flop, three stacked transistors are there i.e. MN1, MN2, and MN3.A feedback signal ha given to MN3 through gate to control the circuit. This circuit diagram, we have implemented both in cadence as well as micro-wind.

Static CDFF

Figure 3 shows a similar P-FF design (SCDFF) using a static conditional discharge technique. It differs from the CDFF design in using a static latch structure. Node *X* is thus exempted from periodical pre-charges. It exhibits a longer data-to-Q (D-to-Q) delay than the CDFF design. The circuit design having delay caused by discharging path which consists of three stacked transistors i.e MN1-MN3.Thats why to overcome for better speed performance and delay a powerful pull-down circuitry is needed and that causes power consumption and extra circuit layout.

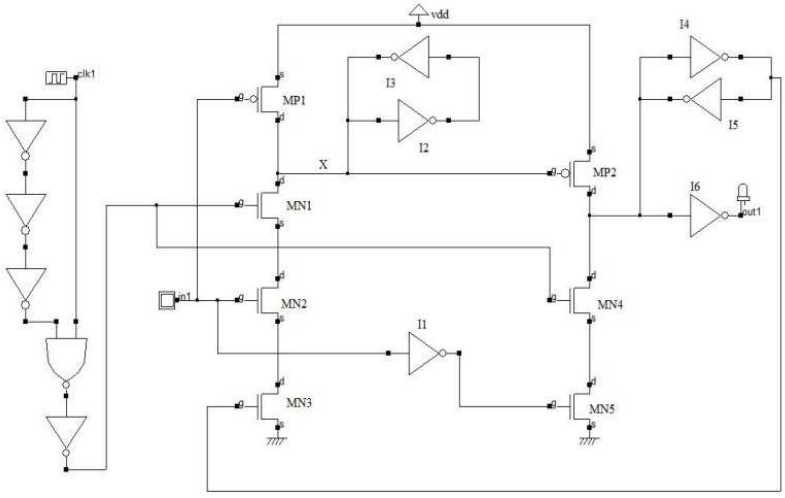

Figure 3: Circuit in Static CDFF

Modified Hybrid Latch Flip-Flop (MHLFF)

The modified hybrid latch flip-flop (MHLFF) shown in Figure 4 which is used as a static latch. The logic of node x is removed. The output signal q is controlled by weak pull-up transistor and maintain the node level x when q=0. At first, the node x is not pre discharged and delay is expected from 0 to 1. The delay decreases further due to level triggered clock pulse is applied to MN3, which is discharged in nature. In this MHLFF, the node transitions occur only when input has different logic value in two successive clocks [3].

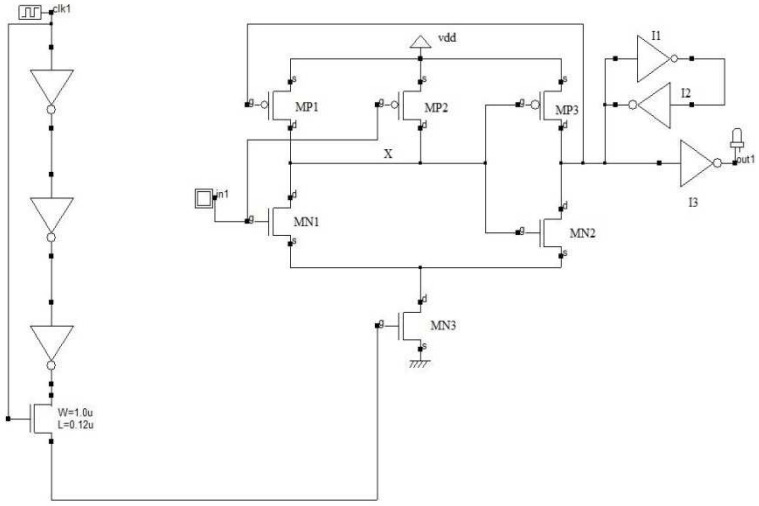

Figure 4: Circuit in MHLFF

Proposed P-FF Design

The proposed design signal feed through a technique which improves and reduce the delay. First MP1 is the 1st weak pull-up transistor, which is used in 1st stage of TSPC latch and gives rise to pseudo-nMos logic design and internal node x is saved for charger keeper and reduces the load capacitance of node X. Next a pass transistor MNx is controlled by the pulse clock. A newly employed, pass transistor MNx provides a discharging path. The work of MNx is to provide extra driving to q node during data transition from 0 to 1 and discharging happening during 1 to 0 data transition. The extra component is n-Mos pass transistor, which is reduced to support the signal feed through a scheme that improves the delay from o to 1

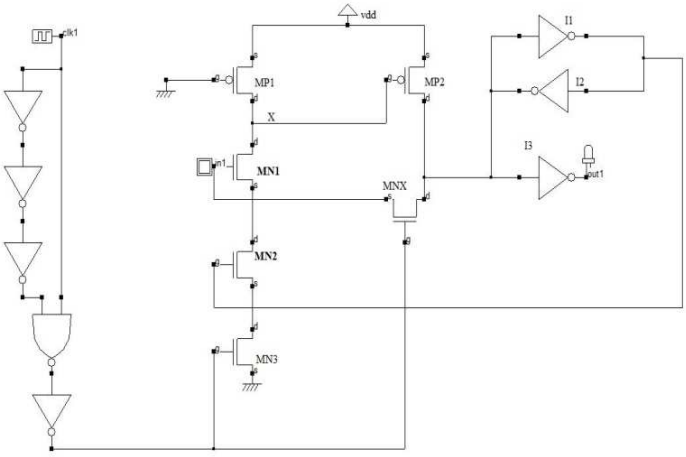

Figure 5: Circuit in Proposed FF

Proposed Efficient Pulse Trigger-Flip Flop

After studying all the circuit we have proposed a new design that is efficient pulse triggered flip-flop (EPTFF) design adopts a signal feed-through technique to improve this delay. Similar to the proposed flip-flop design, the design also has been implemented as a static latch structure and a conditional discharge scheme to avoid switching at an internal node. Here also MP1 with gate connected to the ground which is used in the first stage of the TSPC latch. This is a type of pseudo-nMOS logic style, design, and Figure 6 Efficient PT-FF Design the charge keeper circuit for the internal node *X* can be saved. The circuit also reduces the load capacitance of node *X*. Pass transistor MNx controlled by the pulse clock MP2 is the pull-up transistor at the second stage inverter of the TSPC latch, this extra passage facilitates auxiliary signal driving from the input source to node Q. The level of a node quickly pulled up to shorten the data transition delay. A pass transistor MNx provides a discharging path which having twofold, providing extra driving to node Q during 0 to 1 data transitions, and discharging node Q during "1" to "0" data transitions. The only extra component introduced is an nMOS pass transistor to support the signal feed through. The scheme improves 0 to 1 delay and reduces the difference between the rising time and falling time delay.

When a clock pulse arrives, if no data transition occurs, i.e. in node q, input data and the current passes through the c-Mos pass transistor (MNx) that keeps the input stage of flip-flop away from driving effect. Therefore, no signal switching occurs in any internal nodes. On the other hand, if a "0" to "1" data transition occurs if the node *X* is discharged to turn on transistor MP2, which then pulls node Q high. Here, an inverter is there before mp2, so that it affects the switching operation so that it reduces the power in the whole circuit. Transistor MN3 is controlled by feedback circuit pull-down path of node *X* is off.

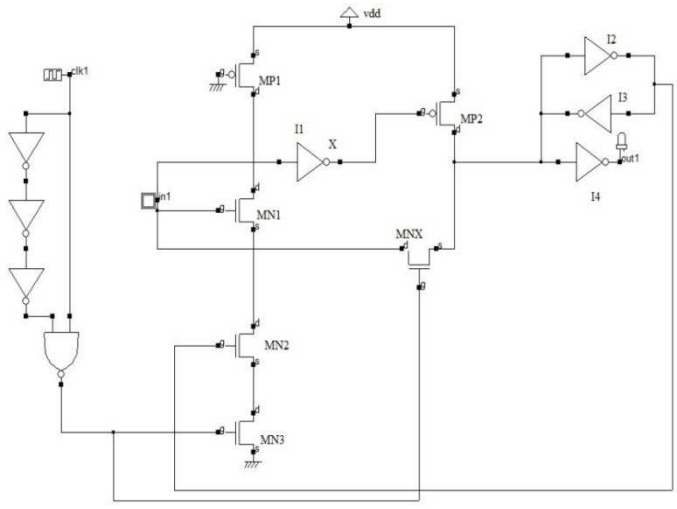

Figure 6: Circuit in EPTFF

All the circuits studied here were implemented using Cadence Virtuoso and their layouts were generated using Micro wind. From these implementations, we could calculate the power, area, delay etc.

We got the simulation output from a layout diagram where we have got maximum current of various circuits from which are given from our experiment and observation.

Comparative Study of Different Edge Trigger Flip Flop Configurations

The Table 1 gives the comparison between different parameters of the flip flop as seen from the timing diagrams.

Table 1: Comparison between Different Configurations of Flip Flop by Using Timing Diagram

Flip-Flop Designs	EP-DCO[2]	CDFF[2]	SCDFF[1]	MHLFF[3]	PFF[1]	EPTFF [Proposed]
I(mA)	**5.0**	**5.0**	**1.0**	**1.0**	**5.0**	**5.0**
I_{MAX} (mA)	0.810	0.810	0.500	0.500	1.214	0.928
Power(mV)	0.005	0.011	0.008	0.004	0.283	0.007
Setup time(ns)	14.6	3.4	4.1	9.9	10.6	10.3
Hold time(ns)	4	9.2	6.5	6	6	2

From the above table we see that the highest maximum current 1.214 mA and lowest 0.500 mA. Here the maximum power obtained is 0.283 mV and the minimum power is 0.004 mV.

After converting from circuit diagram to layout diagram we have calculated area of each circuit which is tabulated in given below. The Table 2 gives the comparison between different parameters of the flip flop

Table 2: Area Calculation of Various Type Flip-Flops

Flip-Flop Designs	λ Value (μm)	No. of Blocks in Horizontal Axis	Horizontal axis(length) =(λ × no. of blocks)[A]	No. of Blocks in Vertical Axis	Vertical axis (breath) = (λ× no. of blocks)[B]	Area (μm^2) =A×B
EP-DCO[1]	0.300	76	22.8	28	8.4	191.52
CDFF[1]	0.600	45	27	15	9	243
SCDFF[3]	0.600	42	25.2	13	7.8	196.56
MHLFF[3]	0.300	71	21.3	27	8.1	172
PFF[3]	0.300	69	20.7	26	7.8	161.46
EPTFF [Proposed]	0.300	68	20.4	27	8.1	165.24

From the above able, we see that what we have newly designed efficient pulse trigger flip-flop we got area 165.25 μm^2 but not better than of proposed flip-flop which having 161.46 μm^2

After observing the simulation of all the circuits, we have extracted various parameter of different circuit which are listed in Table 3, which gives the comparison between different parameters of the flip flop as seen from Voltage Vs Time Plot and Voltage vs. current Plot

Table 3: Comparative Study of Parameters Various Flip-Flop

Flip-Flop Designs	EP-DCO [1]	CDFF [1]	SCDFF [3]	MHLFF [3]	Proposed FF [3]	EPTFF
Power(μw)	11.859	18.162	17.965	10.429	14.595	11.944
Delay (ns)	0.023	0.018	0.018	0.023	0.018	0.013
I_{max} (mA)	0.535	0.701	0.736	0.483	0.736	0.482
No.of transistors	28	30	31	19	24	24
No of nodes	9	9	9	9	6	6
Area($\mu m2$)	191.52	243	196.56	172	161.46	165.24

From above table, we have taken two parameters i.e power and delay of each circuit then we have multiplied of those parameters and got power delay product which is shown bar chat

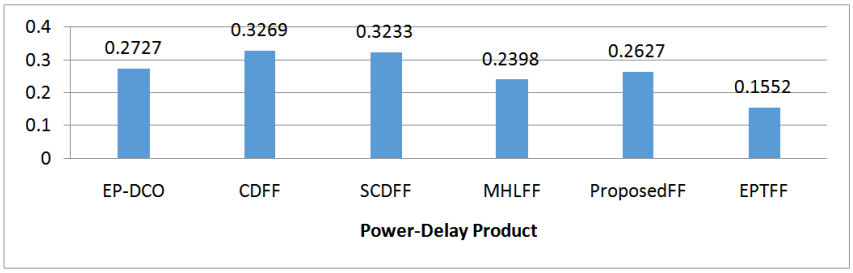

Figure 7: Comparative Study in Power-Delay Product of Various Flip-Flops

CONCLUSIONS

In this paper, we have presented an efficient PT-FF design by employing a modified TSPC structure incorporating a mixed design style, consisting of pass transistor and pseudo n-OS logic. In this study, we have gone through numbers of flip-flops and found out their area, power, delay, setup time, hold time etc. We here have proposed new, efficient flip-flop design which we saw gave better performance especially power and delay which were found out to be 22 mA and 32 ns. We saw that the power delay product has reduced a lot. The power consumption effectively reduced to 11.944μw.

Also, it is showing it's of the area in 165.24μm^2.

We started our study by implementing the EPDCO FF which resulted in a Power of 11.859 μw, Maximum Current 0.535 mA and Area of 191.52 μm^2. In order to get better parameter values, we then went on to implement the CDFF configuration for which we got better results in delay that is 0.023 ns but its area is highly increased to 243.

Next, we observed another circuit that is static-CDFF where the delay is same as we got in previous circuit i.e. CDFF. In case of static-CDFF some improves observed in case of power and delay, but it leaks maximum current 0.736 mA.

If we compare between static-CDFF and MHLFF, all the parameters are improved in case of MHLFF except delay. Here, the numbers of transistors are used in 19 while in case of SCDFF circuit; we have implemented 31 numbers of transistors. The minimum transistors are implemented only in MHLLF i.e. the unique advantage of this circuit.

In case of proposed flip-flop, the numbers of nodes effectively reduced to 6 ,where the numbers of nodes are there same, i.e. 9 in case of ep-DCO, CDFF, static-CDFF. In case of proposed Flip-Flop, Static-CDFF & CDFF the delay is same 0.018 ns. In both proposed Flip-Flop & Static-CDFF, same current flowing in the circuit that is Imax 0.736 mA.

FUTURE WORK

We have improved limited parameter in our efficient pulse trigger design, but simultaneously improve all the parameters are the greatest changelings nowadays. Signal feed through scheme one of them to reduce the power consumption, apart from this other technique also implemented. In this work, we have considered only the Positive Edge Triggered Flip Flop for our study and so study of Negative Edge Triggered Flip Flop may be taken up in the future and a comparative study may be done. The applications of EPTFF were not explored in this paper and may be taken up as an extended work. Moreover, real time signal can be fed to our circuit and their behaviour may be studied as a future work. The glitch reduction, leakage current reduction and addition of delay element some other technique can be implemented to reduce the power-delay product.

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